a programming arrangement entering an identifier into an area of the memory arrangement to be at least one of erased and programmed, the identifier identifying a correct at least one of erasing and programming of the memory arrangement, the programming arrangement altering the identifier in the memory arrangement before at least one of erasing and programming the information.

26. (Amended) The device according to Claim 24, wherein the identifier is altered by at least one of erasing and programming.

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27. (Twice amended) A device, comprising:

a reprogramming arrangement reprogramming information in a memory arrangement of a computer, the reprogramming arrangement selecting an identifier from the information entered into an area of the memory arrangement to be at least one of erased and programmed, the identifier identifying a correct at least one of erasing and programming of the memory arrangement.

REMARKS

Claims 1-32 stand rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the applicant regards as the invention. Specifically, the Office Action identifies the phrase "and/or" as rendering the Claims indefinite "because it is unclear whether the Applicant is claiming one or more of the limitations following the phrase." The Claims have been amended to remove the phrase "and/or."

The Office Action additionally asserts:

> the specification does not support erasing and/or programming. The specification supports a system including a flash device which performs erasing. The same system is disclosed with a different flash device which performs only programming and the same system is disclosed with a different flash device which performs erasing and programming, however, one system including all three embodiments is not supported.

This is not a correct assertion. First, it is well understood in the art that an EPROM (Erasable Programmable Read Only Memory) can be both erased and programmed. Additionally, it is well understood that these operations can occur independent of one another or in sequence. Thus, an EPROM can be erased, programmed, or both erased and programmed. As acknowledged by the Office Action, the Specification does support at least

a flash EPROM that performs both erasing and programming. Therefore the Specification does support a system having a memory that can be erased, programmed, or both erased and programmed. Additionally, the Specification states:

> Memory 104 is an erasable nonvolatile memory, e.g., a flash EPROM memory. A plurality of flash EPROMs which differ greatly with regard to erasing and/or programming may be used here. For example, a first type of flash EPROM 104 must be completely erased before reprogramming. A second type of flash EPROM 104 may be erased and/or programmed in blocks, for example. A third type of flash EPROM may be programmed in pages, for example but no explicit erasing is necessary. (Specification, p. 4, ll. 14 - 20).

In each of the above examples, each EPROM is capable of being erased, programmed, or both erased and programmed. In the third example, erasure is not necessary before reprogramming, but that does not mean that the device is incapable of being erased. It is specifically stated to be an EPROM, which means that it can be erased. Moreover, the description of the second type states that it "**may be erased and/or programmed** in blocks." Thus, this description alone provides at least the necessary support which the Office Action asserts is missing. Furthermore, the Specification additionally states:

> In addition to nonvolatile memory 104, another nonvolatile memory 108 may also be provided. It is possible to use a nonerasable read-only ROM, and an erasable nonvolatile memory in the form of an EPROM, in particular another flash ROM may also be used. It should be pointed out here again that **any arrangement and use of the memory building blocks are possible, and the number of memory building blocks may also be reduced or increased. Only one programmable and/or erasable nonvolatile or refreshable memory, shown here in the form of element 104, is necessary to illustrate the present invention.** (Specification, p. 4, ll. 20 - 27, *emphasis added*).

Thus, the Specification does support a system with multiple EPROMs with differing capabilities and features. Since the Claims have been amended to remove the objectionable phrase "and/or," and since the Specification clearly supports at least one system with the three memory embodiments noted by the Office Action, it is respectfully requested that this rejection of Claims 1-32 under § 112, second paragraph, be withdrawn.

Claims 1-3, 12-14, 24-26 and 27-32 stand rejected under 35 U.S.C. §103(a) as being unpatentable over United States Patent No. 5,930,826 to Lee et al. ("the Lee reference").[1] The rejection should be withdrawn for at least the following reasons.

Three basic criteria must be met to establish a *prima facie* case of obviousness. First, the prior art references must teach or suggest all the claim limitations. Second, the

references or the knowledge generally available to one of ordinary skill in the art must provide some suggestion or motivation to modify the reference or to combine reference teachings. Third, there must be a reasonable expectation of success. M.P.E.P. § 2143.

The Office Action provides the following argument in support of the rejection:

> Regarding Applicants' argument that Lee does not teach providing an identifier identifying a correct erasing and/or programming of an area in memory arrangement, the Examiner disagrees. Lee teaches that the identifier(s) are protection bits which prevent the corresponding data from being erased, programmed or read incorrectly (C 2, L 42-48;C 3, L 40-64; C 4, L 1-48) and thus the identifier in Lee's system does identify a correct erasing and/or programming memory arrangement. When the erase and/or program bits of the identifier indicate an unprotected state, the corresponding data is correct erasing and/or programming memory arrangement. **The phrase "correct erasing and/or programming" is interpreted to mean an approved area to erase or program."** (*emphasis added*)

The Applicants disagree with the Office's "interpretation" of the phrase "correct erasing and/or programming." The meaning of this phrase is clearly described throughout Specification, for example:

> The method and the respective device serve to secure the functionality of a control unit, for example, when an interruption or malfunction has occurred during erasing and/or programming. To do so, when an interruption or a reset occurs during erasing or programming or when the device otherwise becomes de-energized, this is noted in a memory device, in particular in the memory device to be programmed. **In addition, in programming an identifier that identifies correct erasing and/or programming of the memory is entered into an area of the memory that is to be erased and/or programmed later**, in particular an area that is to be erased and/or programmed last, **and this identifier is altered before erasing or programming the data or programs in such a way that the program is not executed if programming is incomplete and/or the data is not used if data entry is not complete.** Thus, an error in programming or erasing can be corrected after a possible data modification.
>
> Advantageously, **the expected identifier that identifies the completeness and accuracy of the programming** is used as part of the program, in particular as part of the program identifier itself, and consequently does not take up any additional memory. (Specification, p. 3, l. 23 – p. 4, l. 6, *emphasis added*).

Thus, "correct erasing and/or programming" as used in the present application means that an erasing and/or programming operation has been completed correctly.

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[1] The Office Action discussion under this rejection also includes reference to Claims 4-6, and 15-18. Applicants have included corresponding discussion of each of these Claims in this Amendment.

The Lee reference describes PGM-bit, ERS-bit, and RD-bit, which are protection bits that prevent programming, erasing, and reading, respectively, of an area of memory when they are set. They do not indicate whether such operations were completed correctly. Therefore, the Lee reference does not disclose an "identifier identifying a correct at least one of erasing and programming of the memory arrangement," as recited in amended Claim1.

Furthermore, attempting to use the protection bits as an identifier recited in Claim 1, as suggested by the Office Action, would prevent the Lee system from operating properly. Claim 1 states:

> A method of at least one of erasing and programming information in a memory arrangement of a computer, comprising the steps of:
>
> providing an identifier into an area of the memory arrangement that is to be at least one of erased and programmed, the identifier identifying a correct at least one of erasing and programming of the memory arrangement; and
>
> **altering the identifier in the memory arrangement before at least one of erasing and programming.**

The Lee reference states:

> The protection information of each memory sector is stored in the protection bit array 11. The protection bit array 11 comprises three bits of information, i.e., **ERS-bit 81, PGM-bit 82 and RD-bit 83, for indicating the protection state of erase, program, and read operations** respectively for each sector. The data of a sector are read to a memory sense amplifier 13, and the protection bits are read to a protection sense amplifier 14, respectively. Before any further operation on the data of the selected sector is executed, the corresponding protection bit is examined first. **If it shows that the selected sector is protected, the operation will be terminated.** (Lee, col. 3, ll. 50-64, *emphasis added*).

Thus, applying the argument asserted in the Office Action, the following would result from applying Lee to Claim 1:

1) The PGM-bit would identify a correct programming of an area in memory. That is, when PGM-bit is set, the area is approved to be programmed and when not set, the area is not approved.
2) PGM-bit is set and provided into an area of memory identifying a correct programming the memory (approved for programming).
3) The PGM-bit is altered (cleared – not set) before programming or erasing the memory.

Since the PGM-bit only has two states, altering a set PGM-bit causes it to be cleared or not set. When the PGM-bit is not set, it indicates a protected state. Thus, according to the Lee reference, subsequent attempt to program the area of memory would be terminated. (Lee, col. 3, ll. 50-64). Therefore, using the PGM-bit as the identifier recited in Claim 1 would prevent the Lee system from being able to program the area of memory. The ERB-bit operates with the erase function in the same way as the PGM-bit does for the program function, and the erase function would likewise fail to operate according to Claim 1. Thus, using the protection bits described in the Lee reference as the identifier recited in Claim 1 would render the system inoperable. Therefore, the Lee reference not only fails to disclose each and every element of Claim 1, it actually teaches away from the invention of Claim1.

For the foregoing reasons, the Lee reference fails to render Claim 1 or its dependent Claims 2-6 obvious under 35 U.S.C. §103(a). Since Claims 12, 24 and 27 include a similar limitation regarding an identifier identifying a correct at least one of programming and erasing of the memory arrangement, the Lee reference also does not render Claims 12, 24 and 27 or their dependent Claims 13-18, 25-26, and 28-32 obvious under 35 U.S.C. §103(a). Therefore, it is respectfully requested that this rejection be withdrawn.

Claims 7-11 and 19-23 stand rejected under 35 U.S.C. §103(a) as being unpatentable over the Lee reference in view of Japanese Patent 09161493 to Yousuke et al. ("the Yousuke reference"). As described above, the Lee reference does not disclose the limitation regarding an identifier that "identifies a correct programming and erasing of the memory arrangement," and further teaches away from using protection bits as the identifier. The Yousuke reference also does not disclose this limitation. According to the Office Action:

> Yousuke is not provided in the rejection to suggest modifying Lee to include an identifier identifying a correct erasing and/or programming area of memory arrangement as this feature is already taught by Lee.

Since the Yousuke reference is not provided to, and does not, suggest modifying Lee to include an identifier identifying a correct erasing and/or programming area of memory arrangement, and since the Lee reference does not teach or suggest an identifier that can function as recited in the pending independent Claims 1 and 12, the Lee and Yousuke reference do not teach or suggest each and every limitation of the pending Claims 7-11 and 19-23 dependent from Claims 1 and 12. Therefore, the Lee and Yousuke references cannot render Claims 7-11 and 19-23 obvious under 35 U.S.C. §103(a). It is therefore respectfully requested that this rejection be withdrawn.

CONCLUSION

In light of the foregoing, Applicants respectfully submit that all of the pending claims are in condition for allowance. Prompt reconsideration and allowance of the present application are therefore earnestly solicited.

Respectfully Submitted,

Dated: 12/19/02

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AMENDMENT VERSION WITH MARKUP

In the Claims:

1. (Twice amended) A method of at least one of erasing and programming[erasing and/or programming] information in a memory arrangement of a computer, comprising the steps of:

providing an identifier into an area of the memory arrangement that is to be at least one of erased and programmed[erased and/or programmed], the identifier identifying a correct at least one of erasing and programming[erasing and/or programming] of the memory arrangement; and

altering the identifier in the memory arrangement before at least one of erasing and programming[erasing and/or programming] the information.

3. (Amended) The method according to Claim 1, wherein the altering step includes the substep of:

altering the identifier by at least one of erasing and programming[erasing and/or programming].

4. (Amended) The method according to Claim 1, further comprising the step of:

entering the identifier into a further area of the memory arrangement, the further area being at least one of erased and programmed[erased and/or programmed] only after at least one of erasing and programming[erasing and/or programming] of the area.

5. (Amended) The method according to Claim 4, wherein the further area is to be at least one of erased and programmed[erased and/or programmed] last.

7. (Amended) The method according to Claim 1, further comprising the step of:

altering the identifier by at least one of erasing and programming[erasing and/or programming] so that the identifier is unidentifiable.

9. (Amended) The method according to Claim 1, further comprising the step of:

checking the identifier after at least one of (a) an interruption in at least one of erasing and programming[erasing and/or programming] and (b) at least one of erasing and programming[erasing and/or programming] the memory arrangement.

11. (Amended) The method according to Claim 10, further comprising the steps of:

checking at least one of the identifier and the flag before at least one of erasing and programming[erasing and/or programming]; and

analyzing at least one of the identifier and the flag before at least one of erasing and programming[erasing and/or programming].

12. (Twice amended) A method of reprogramming information in a memory arrangement of a computer, comprising the step of:

selecting an identifier from the information entered into an area of the memory to be at least one of erased and programmed[erased and/or programmed], the identifier identifying a correct at least one of erasing and programming[erasing and/or programming] of the memory arrangement.

14. (Twice amended) The method according to claim 12, further comprising the step of:

selecting the identifier from the information entered into a further area of the memory arrangement, the further area being at least one of erased and programmed[erased and/or programmed] only after at least one of erasing and programming[erasing and/or programming] of the area.

15. (Amended) The method according to Claim 14, wherein the further area is to be at least one of erased and programmed[erased and/or programmed] last.

16. (Twice amended) The method according to claim 12, further comprising the step of:

altering the selected identifier in the memory arrangement before at least one of erasing and programming[erasing and/or programming] the information.

17. (Amended) The method according to Claim 16, wherein the altering step includes the substep of:

altering the selected identifier by at least one of erasing and programming[erasing and/or programming].

19. (Amended) The method according to Claim 12, further comprising the step of:

altering the identifier by at least one of erasing and programming[erasing and/or programming] so that the identifier is unidentifiable.

21. (Amended) The method according to Claim 12, further comprising the step of:

checking the identifier after at least one of (a) an interruption in at least one of erasing and programming[erasing and/or programming] and (b) at least one of erasing and programming[erasing and/or programming] the memory arrangement.

23. (Amended) The method according to Claim 22, further comprising the steps of:

checking at least one of the identifier and the flag before at least one of erasing and programming[erasing and/or programming]; and

analyzing at least one of the identifier and the flag before at least one of erasing and programming[erasing and/or programming].

24. (Twice amended) A device for at least one of erasing and programming[erasing and/or programming] information in a memory arrangement of a computer, comprising:

a programming arrangement entering an identifier into an area of the memory arrangement to be at least one of erased and programmed[erased and/or programmed], the identifier identifying a correct at least one of erasing and programming[erasing and/or programming] of the memory arrangement, the programming arrangement altering the identifier in the memory arrangement before at least one of erasing and programming[erasing and/or programming] the information.

26. (Amended) The device according to Claim 24, wherein the identifier is altered by at least one of erasing and programming[erasing and/or programming].

27. (Twice amended) A device, comprising:

a reprogramming arrangement reprogramming information in a memory arrangement of a computer, the reprogramming arrangement selecting an identifier from the information entered into an area of the memory arrangement to be at least one of erased and programmed[erased and/or programmed], the identifier identifying a correct at least one of erasing and programming[erasing and/or programming] of the memory arrangement.